

- ☐ Tentative Specification
- ☐ Preliminary Specification
- ☒ Approval Specification

MODEL NO.: V420HJ1
SUFFIX: LE6

Customer:	
APPROVED BY _____ Name / Title Note _____ Please return 1 copy for your confirmation with your signature and comments.	SIGNATURE _____

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CONTENTS

CONTENTS	2
1. GENERAL DESCRIPTION.....	5
1.1 OVERVIEW	5
1.2 FEATURES.....	5
1.3 APPLICATION	5
1.4 GENERAL SPECIFICATIONS	5
1.5 MECHANICAL SPECIFICATIONS	6
2. ABSOLUTE MAXIMUM RATINGS	7
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	7
2.2 PACKAGE STORAGE	8
2.3 ELECTRICAL ABSOLUTE RATINGS	8
2.3.1 TFT LCD MODULE.....	8
2.3.2 BACKLIGHT CONVERTER UNIT	8
3. ELECTRICAL CHARACTERISTICS	9
3.1 TFT LCD MODULE.....	9
3.2 BACKLIGHT CONVERTER UNIT	11
3.2.1 LED LIGHT BAR CHARACTERISTICS	11
3.2.2 CONVERTER CHARACTERISTICS.....	11
3.2.3 CONVERTER INTERFACE CHARACTERISTICS.....	12
4. BLOCK DIAGRAM OF INTERFACE	14
4.1 TFT LCD MODULE.....	14
5. INTERFACE PIN CONNECTION	15
5.1 TFT LCD MODULE.....	15
5.2 CONVERTER UNIT.....	18
5.3 LVDS INTERFACE	20
5.4 COLOR DATA INPUT ASSIGNMENT	22
6. INTERFACE TIMING	23
6.1 INPUT SIGNAL TIMING SPECIFICATIONS.....	23
6.2 POWER ON/OFF SEQUENCE	26
7. OPTICAL CHARACTERISTICS	27
7.1 TEST CONDITIONS	27
7.2 OPTICAL SPECIFICATIONS.....	28
8. PRECAUTIONS	31

8.1 ASSEMBLY AND HANDLING PRECAUTIONS	31
8.2 SAFETY PRECAUTIONS	31
9. DEFINITION OF LABELS	32
9.1 CMI MODULE LABEL	32
10. PACKAGING	33
10.1 PACKAGING SPECIFICATIONS	33
10.2 PACKAGING METHOD	33
11. MECHANICAL CHARACTERISTIC	35

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Nov. 08, 2012	All	All	The Approval specification was first issued.
		6	1.5	Modify Module Weight.
		28	7.2	Modify Color Chromaticity (Gy).
		33	10.1	Modify Box dimensions.
		33	10.2	Modify Packing Method.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420HJ1-LE6 is a 42" TFT Liquid Crystal Display module with LED Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The converter module for backlight is built-in.

1.2 FEATURES

- High brightness (350 nits)
- High contrast ratio (5000:1)
- Fast response time (Gray to gray average 9.5 ms)
- High color saturation (NTSC 68%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 50Hz/60Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- Viewing Angle : 176(H)/176(V) (CR ≥ 20) VA Technology
- RoHs compliance
- T-con input frame rate: 50Hz/60Hz, output frame rate: 50Hz/60Hz

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

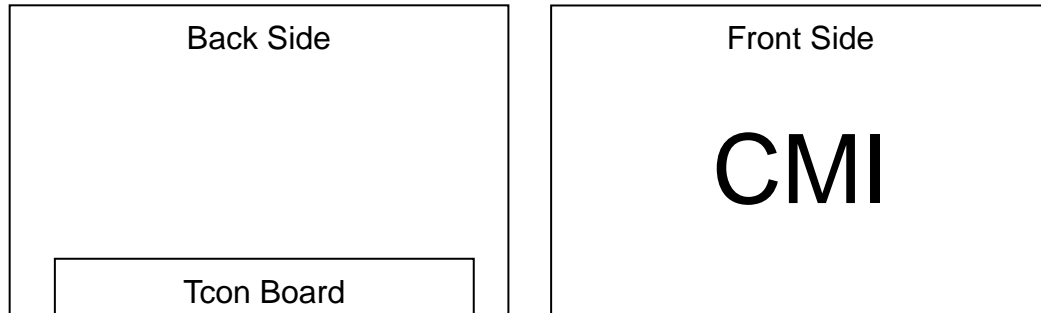
1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24 (H) x 523.26 (V)	mm	(1)
Bezel Opening Area	938.84 (H) x 531.26 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Anti-Glare coating (Haze 1%) Hardness 3H	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with "CMI"		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

Note (3)



1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	949.84	950.84	951.84	mm	(1)
	Vertical (V)	546.26	547.26	548.26	mm	(1)
	Depth (D)	20.1	21.1	22.1	mm	(2)
	Depth (D)	26.7	27.7	28.7	mm	(3)
Weight		8,740	9,200	9,660	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to Converter cover

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40$ °C).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

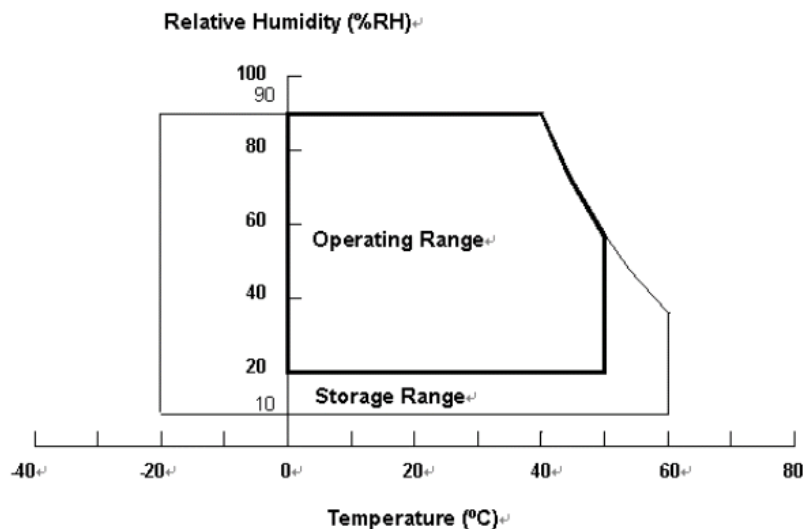
(c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	—	60	VRMS	
Converter Input Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	6	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

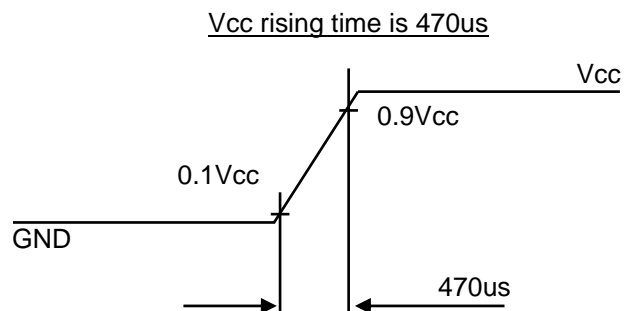
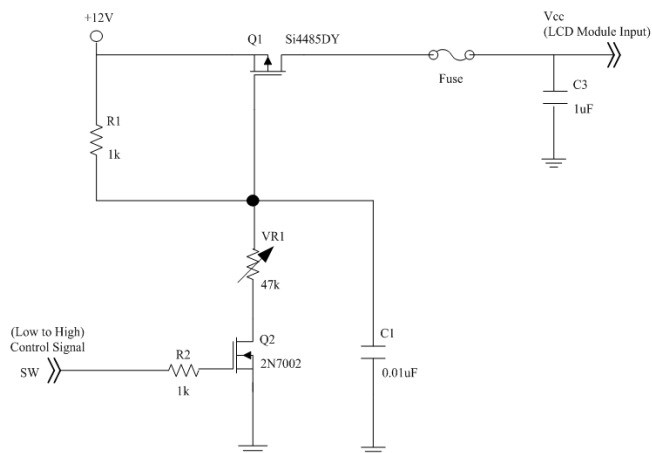
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	-	2.5	A	(2)
Power consumption	White Pattern	P _T	—	3.48	4.52	W	(3)
	Horizontal Stripe	P _T	—	5.88	7.64	W	
	Black Pattern	P _T	—	3.36	4.37	W	
Power Supply Current	White Pattern	—	—	0.29	0.38	A	(3)
	Horizontal Stripe	—	—	0.49	0.64	A	
	Black Pattern	—	—	0.28	0.36	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	+300	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	-300	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

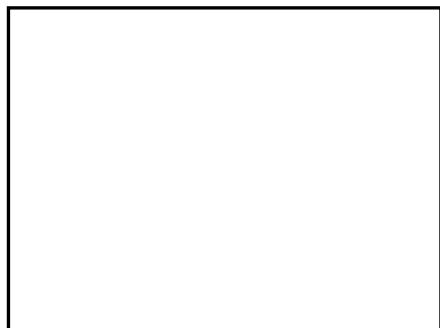
The ripple voltage should be controlled under 10% of V_{CC} (Typ.)

Note (2) Measurement Conditions:



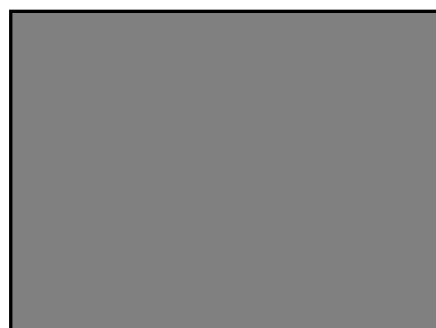
Note (3) The specified power supply current is under the conditions at $V_{CC} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



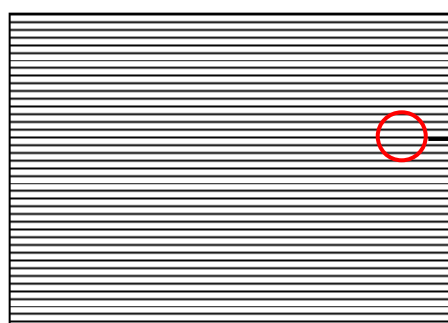
Active Area

b. Black Pattern

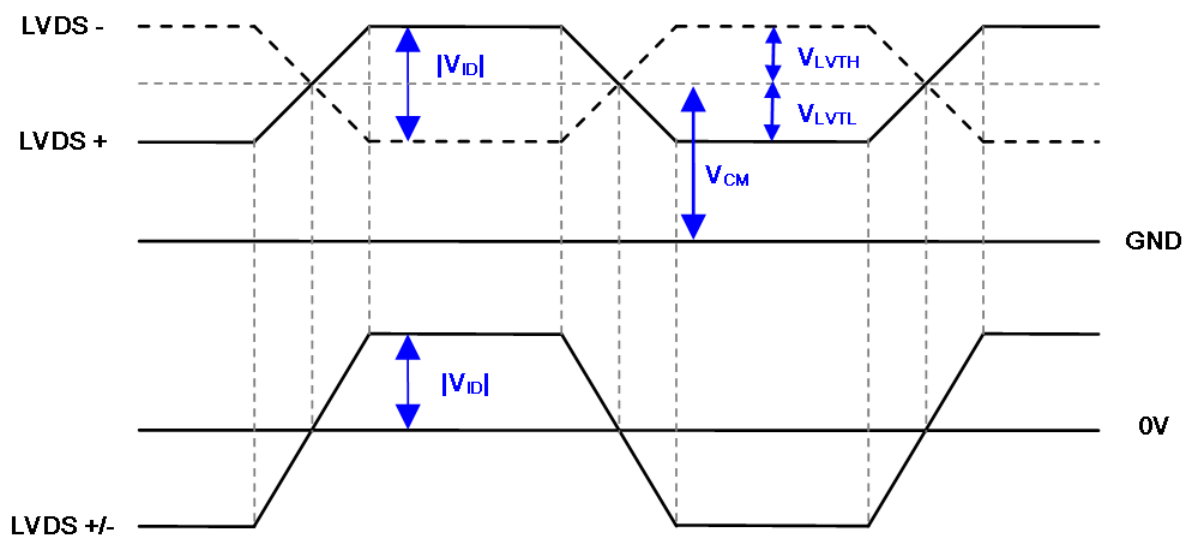


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics is shown as below.



3.2 BACKLIGHT CONVERTER UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS

The backlight unit contains 1 pcs light bar.

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
One String Current	I _L	117.5	125	132.5	mA	
One String Voltage	V _W	33.6	-	38.64	V _{DC}	I _L = 125mA
One String Voltage Variation	ΔV _W	-	-	1	V	
Life time	-	30,000	-	-	Hrs	(1)

Note (1) Dimming Ratio=100%

Note (2) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, IL = 125 mA

3.2.2 CONVERTER CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	40.8	47.04	W	(1), (2), IL = 125 mA
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	I _{BL}	-	1.7	1.96	A	Non Dimming
Input Inrush Current	I _R	-	-	2.65	Apeak	V _{BL} =22.8V, (IL=typ.) (3)
Dimming Frequency	FB	90	160	190	Hz	
Dimming Duty Ratio	DDR	5	-	100	%	(4)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off.

The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 42" backlight unit under input voltage 24V, average LED current 132.5 mA

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) EPWM signal have to input available duty range. 5% minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on	(5)
	LO		—	0	—	0.8	V	Duty off	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open	
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V _{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us		
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ		
PWM Delay Time		TPWM	—	100	—	—	ms		
BLON Delay Time		T _{on}	—	300	—	—	ms		
		T _{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. (Fig.2)

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

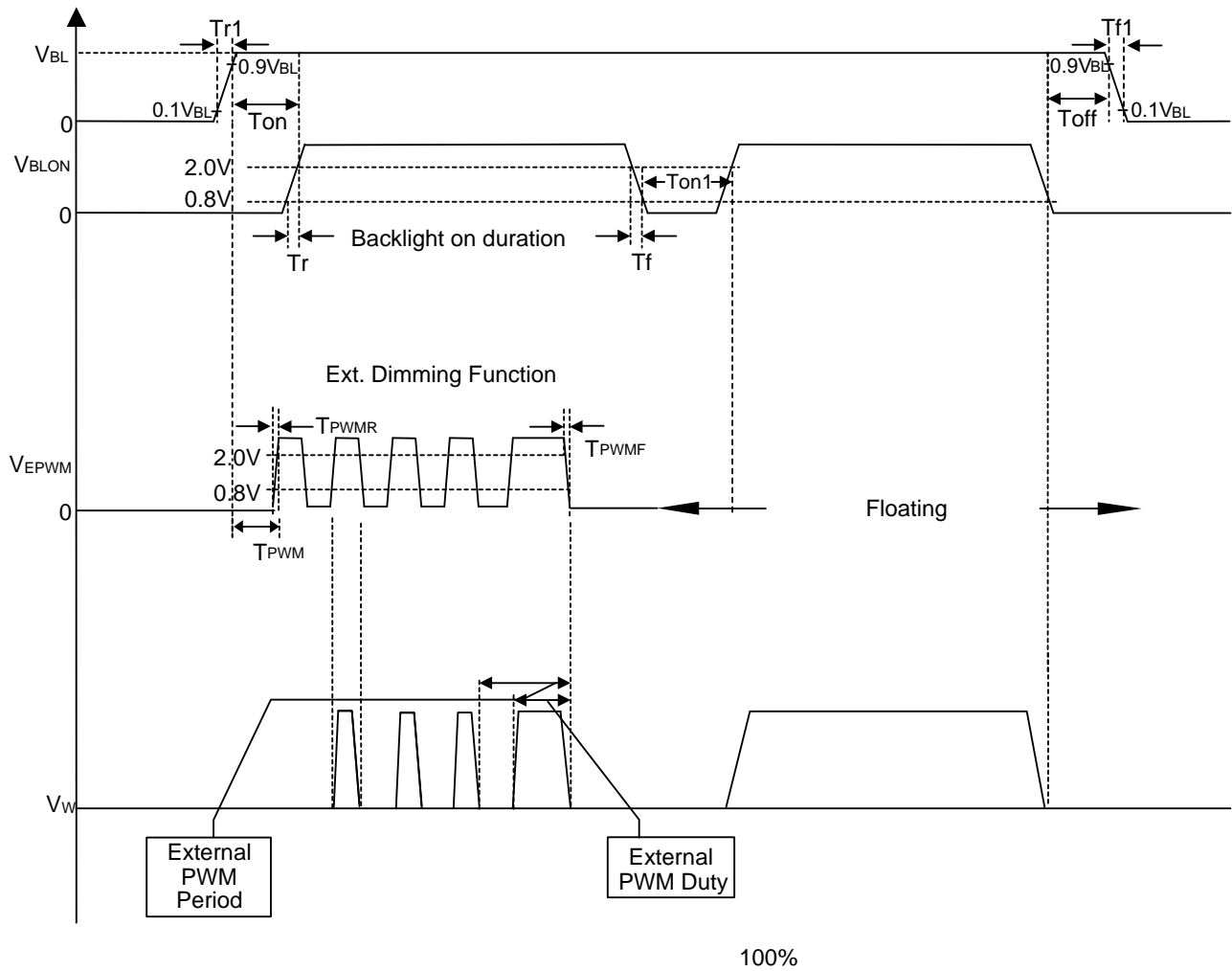


Fig. 1

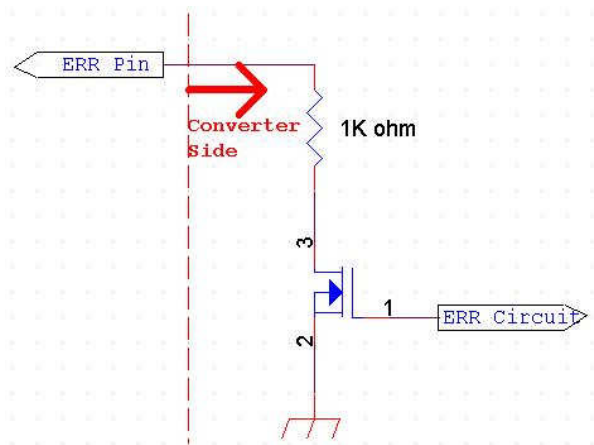


Fig. 2

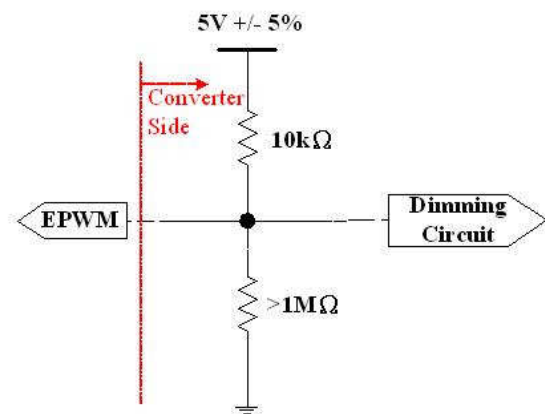
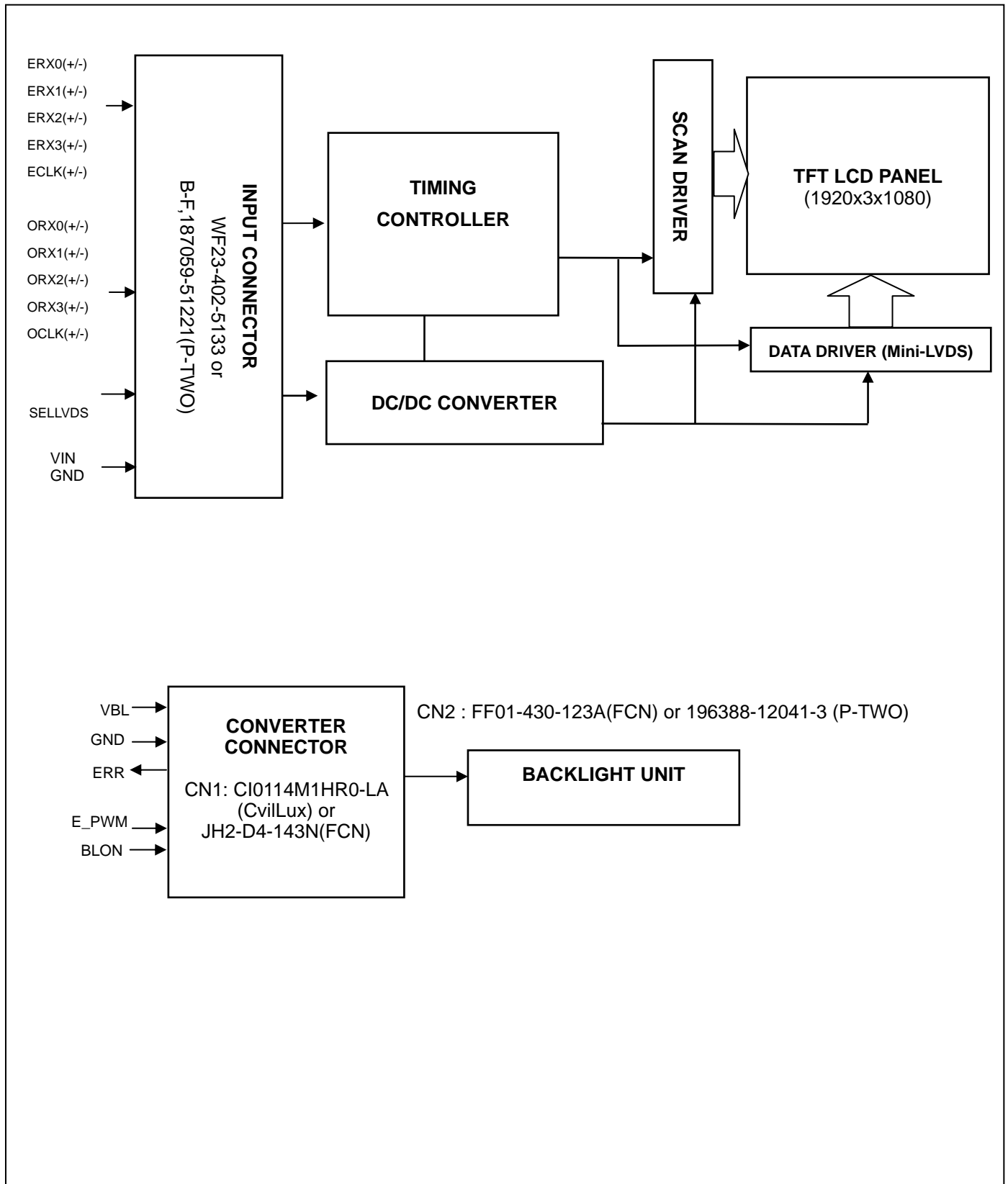


Fig. 3

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

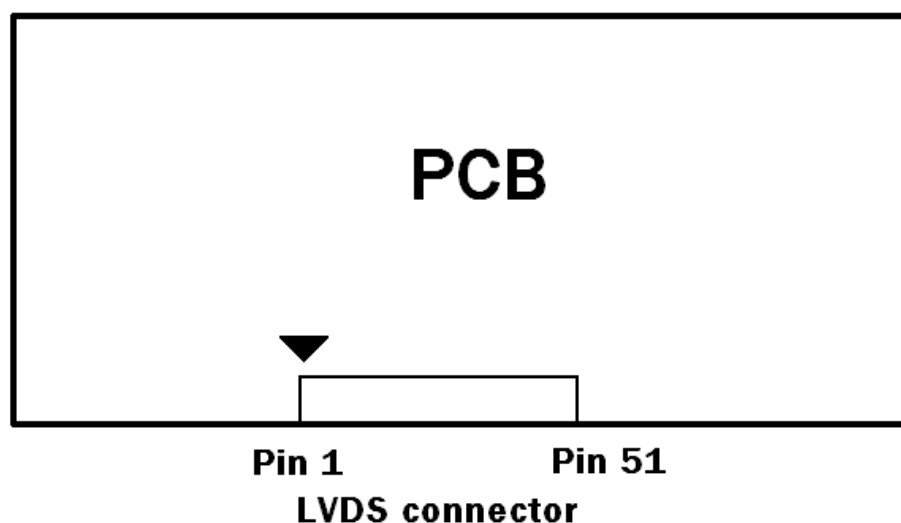
CNF1 Connector Part No.: WF23-402-5133,(FCN) or B-F,187059-51221(P-TWO)

Mating connector: JAE FI-RE51HL

Pin	Name	Description	Note
1	N.C.	No Connection	(2)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(3)(4)
8	N.C.	No Connection	(2)
9	N.C.	No Connection	(2)
10	N.C.	No Connection	(2)
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input.	(5)
20	OCLK+	Odd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(2)
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	

30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input	(5)
36	ECLK+	Even pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	Power input (+12V)	
49	VCC	Power input (+12V)	
50	VCC	Power input (+12V)	
51	VCC	Power input (+12V)	

Note (1) LVDS connector pin order is defined as below.



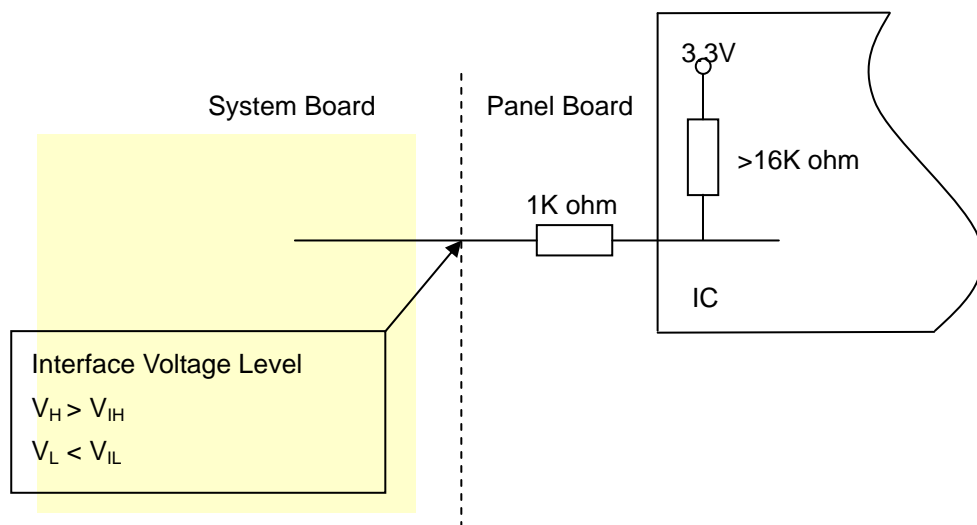
Note (2) Reserved for internal use. Please leave it open.

Note (3)

SELLVDS	Mode
L	JEIDA
H(default)	VESA

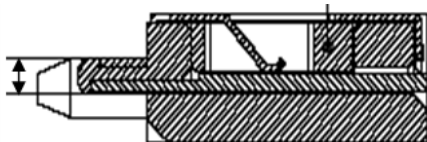
L : Connect to GND, H : Connect to Open or +3.3V

Note (4) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including panel board loading as below.



Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (6) LVDS connector mating dimension range request is 0.93mm~1.0mm as below



5.2 CONVERTER UNIT

CN1(Header): CI0114M1HR0-LA (CvilLux) or JH2-D4-143N(FCN)

Mating connector : JST PHR-14

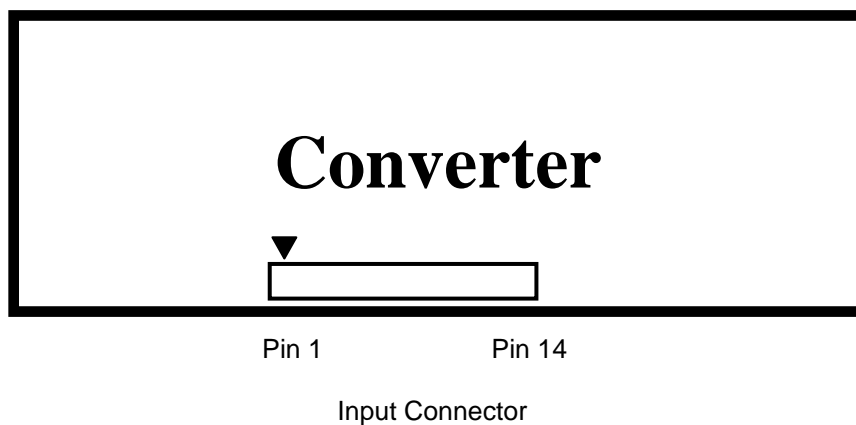
Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

CN2(Header): FF01-430-123A(FCN) or 196388-12041-3 (P-TWO)

Pin No	Symbol	Feature
1	VLED-	Negative of LED String
2	VLED-	
3	VLED-	
4	VLED-	
5	VLED-	
6	VLED-	
7	VLED-	
8	VLED-	
9	NC	NC
10	VLED+	Positive of LED String
11	VLED+	
12	VLED+	

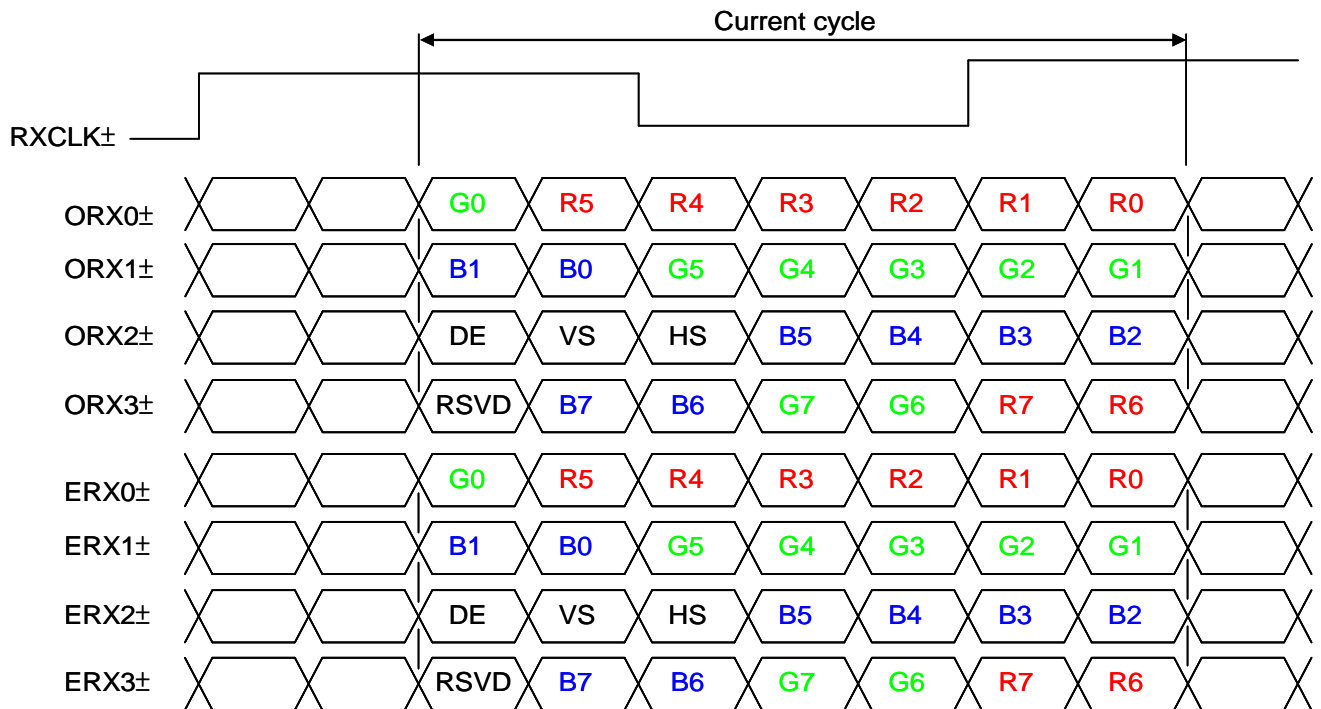
Note (1) If Pin14 is open, E_PWM is 100% duty.

Note (2) Input connector pin order defined as follows

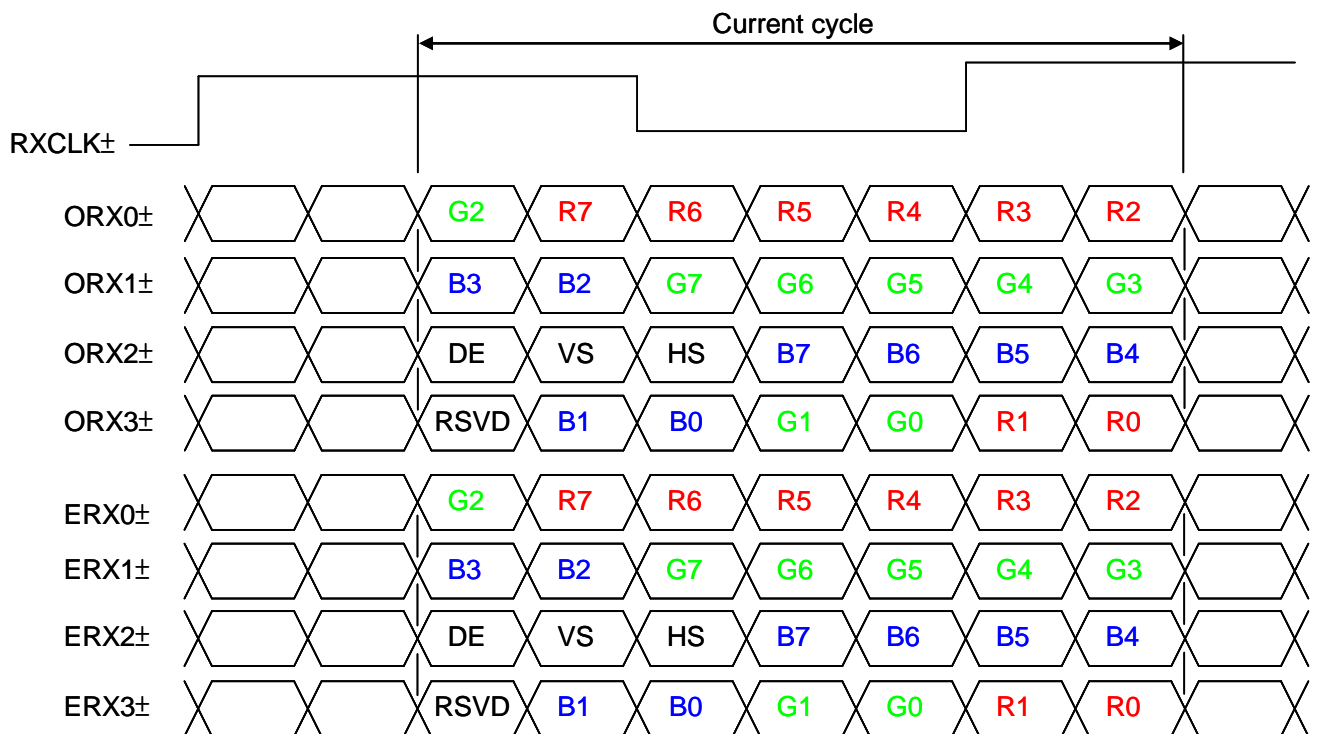


5.3 LVDS INTERFACE

VESA Format : SELLVDS = H or Open



JEIDA Format : SELLVDS = L



R0~R7	Pixel R Data (7; MSB, 0; LSB)	DE	Data enable signal
G0~G7	Pixel G Data (7; MSB, 0; LSB)	DCLK	Data clock signal
B0~B7	Pixel B Data (7; MSB, 0; LSB)		

Note (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

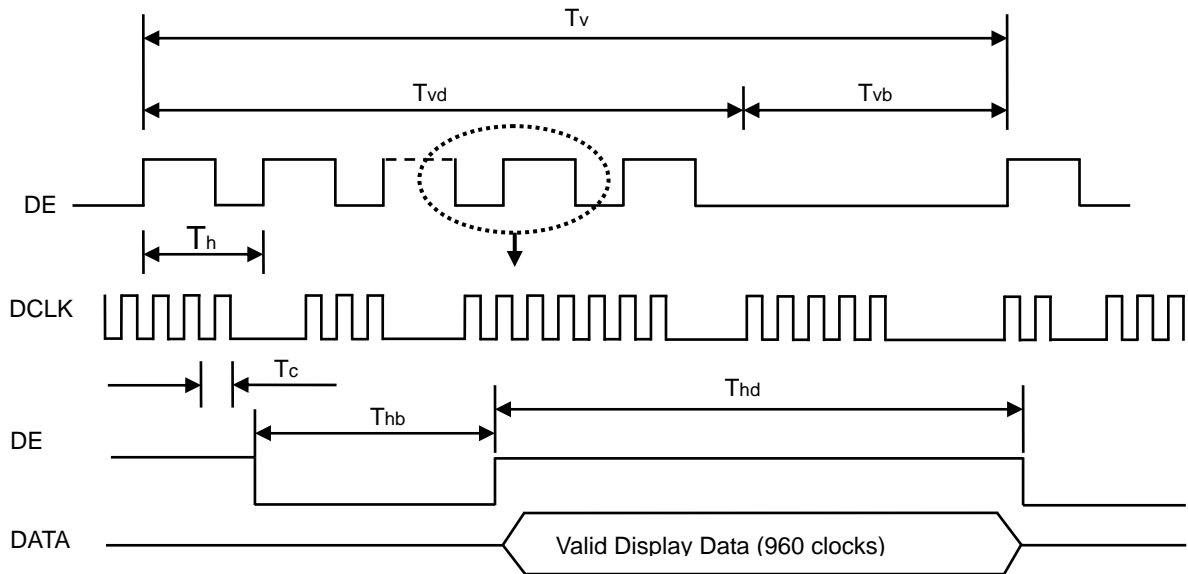
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-2\%$	—	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(5)
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	
		F_{r6}	57	60	63	Hz	
	Total	T_{v}	1090	1125	1480	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
	Display	T_{vd}	1080	1080	1080	Th	
	Blank	T_{vb}	10	45	400	Th	
Horizontal Active Display Term	Total	T_{h}	1030	1100	1325	Tc	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
	Display	T_{hd}	960	960	960	Tc	
	Blank	T_{hb}	70	140	365	Tc	

Note (1) Please make sure the range of frame rate has follow the below equation :

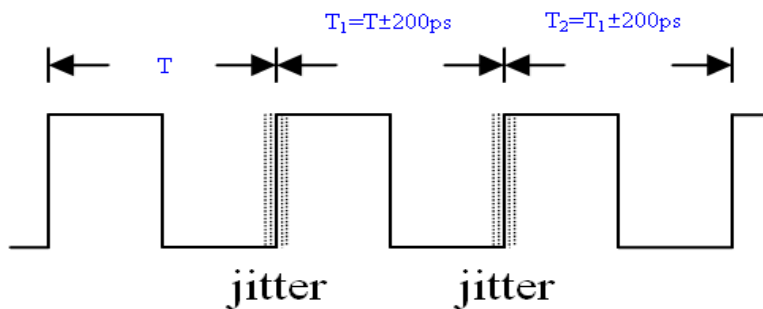
$$F_{\text{clkin}}(\text{max}) \geq F_{\text{r6}} \times T_{\text{v}} \times T_{\text{h}}$$

$$F_{\text{r5}} \times T_{\text{v}} \times T_{\text{h}} \geq F_{\text{clkin}}(\text{min})$$

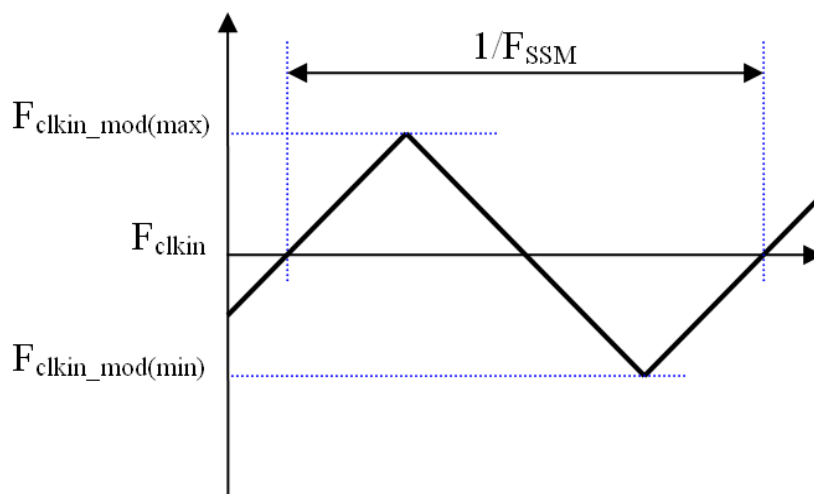
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram as below:



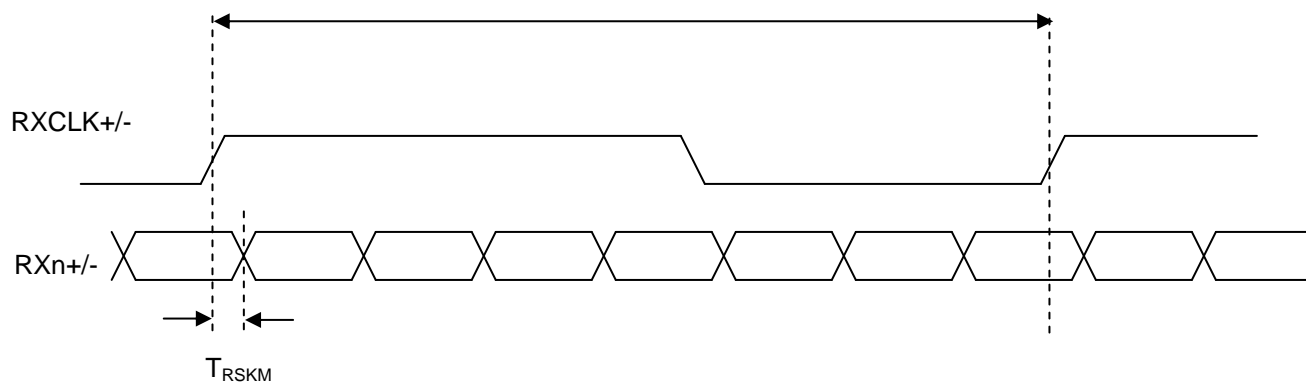
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T|$



Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



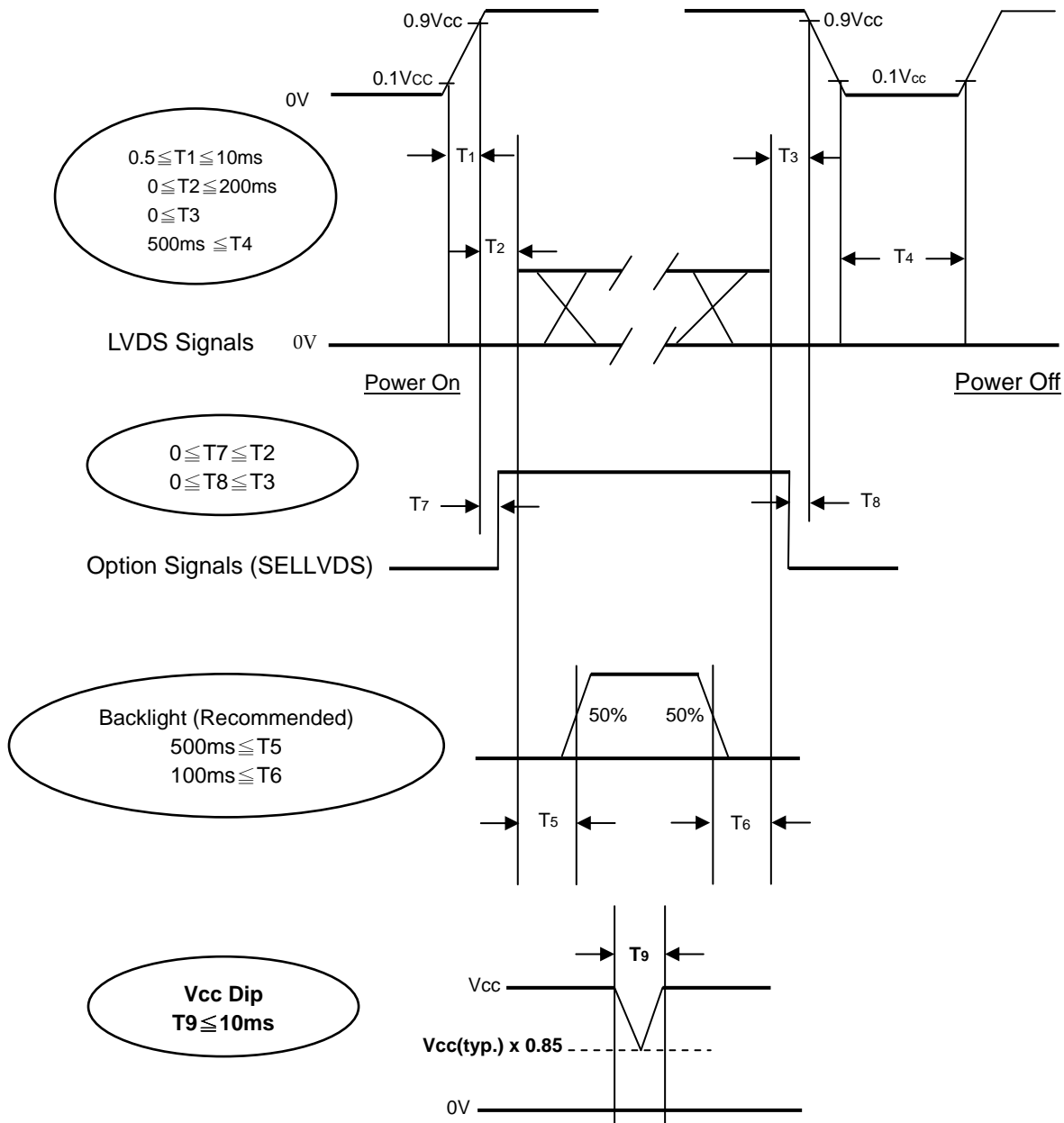
Note (5) The LVDS timing diagram and the receiver skew margin is defined and shown in following figure.



6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

If $T2 < 0$, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

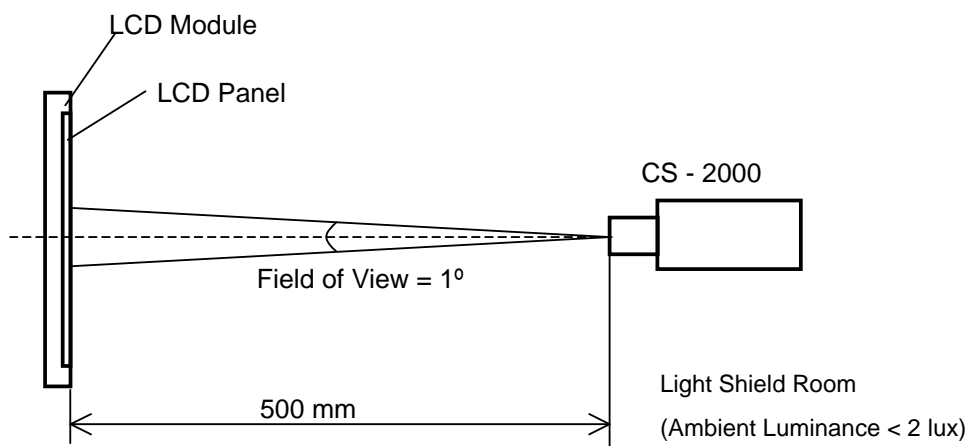
Note (6) Vcc must decay smoothly when power-off.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	125±4	mA
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



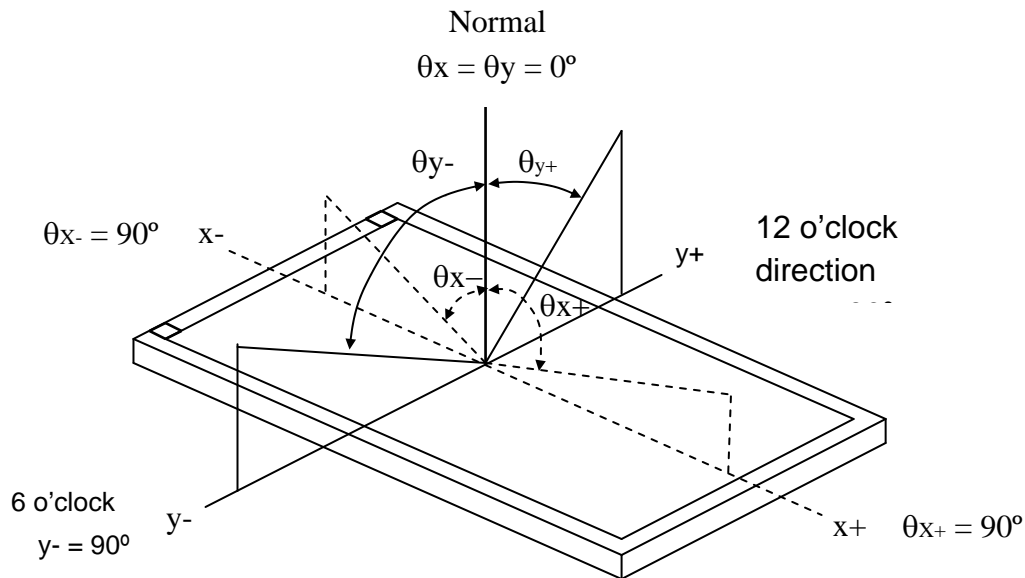
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta x=0^{\circ}, \theta y=0^{\circ}$ Viewing angle at normal direction	4000	5000		-	(2)
Response Time (VA)		Gray to gray			9.5	17	ms	(3)
Center Luminance of White		L _C		280	350		cd/m ²	(4)
White Variation		δW				1.3	-	(6)
Cross Talk		CT				4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.636	Typ. +0.03	-	-
		Ry			0.328		-	
	Green	Gx			0.302		-	
		Gy			0.593		-	
	Blue	Bx			0.150		-	
		By			0.055		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Correlated color temperature				-		10000	
	Color Gamut	C.G.		-	68	-	%	NTSC
	Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.
θx-			80		88	-		
Vertical		θy+	80		88	-		
		θy-	80		88	-		

Note (1) Definition of Viewing Angle (θ_x , θ_y) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

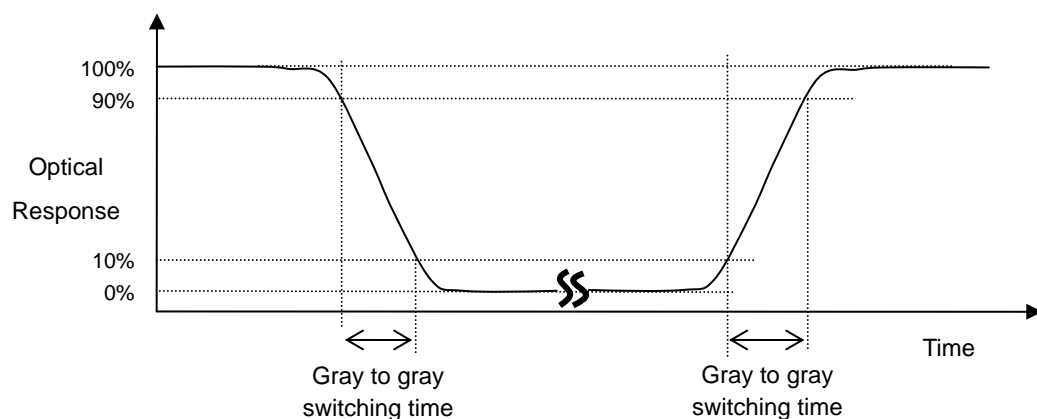
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White (L_C , L_{AVE}) :

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$, where $L(X)$ is corresponding to the luminance of the point X at the figure in Note (6).

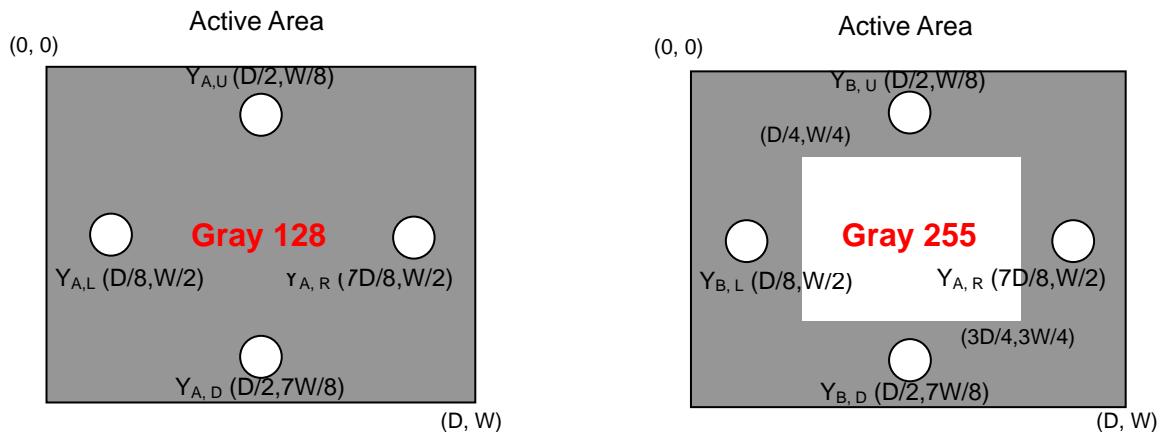
Note (5) Definition of Cross Talk (CT) :

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m²)

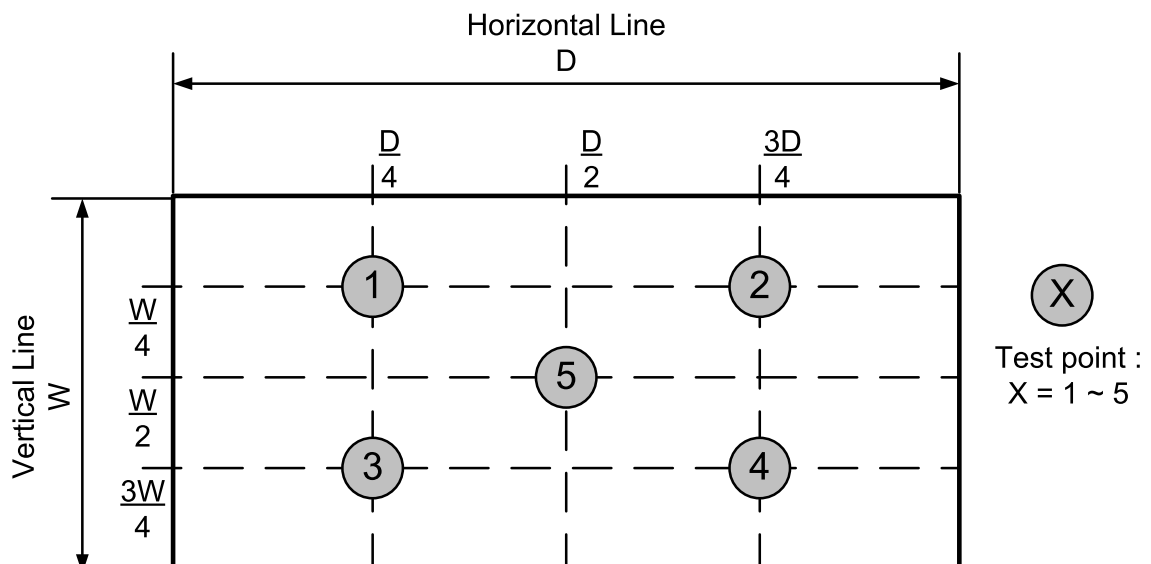
Y_B = Luminance of measured location with gray level 255 pattern (cd/m²)



Note (6) Definition of White Variation (δW) :

Measure the luminance of gray level 255 at 5 points

$$\delta W = \frac{\text{Maximum } [L(1), L(2), L(3), L(4), L(5)]}{\text{Minimum } [L(1), L(2), L(3), L(4), L(5)]}$$



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.
- [5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.
- [6] Do not plug in or pull out the I/F connector while the module is in operation.
- [7] Do not disassemble the module.
- [8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [9] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [10] When storing modules as spares for a long time, the following precaution is necessary.
 - [10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [11] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

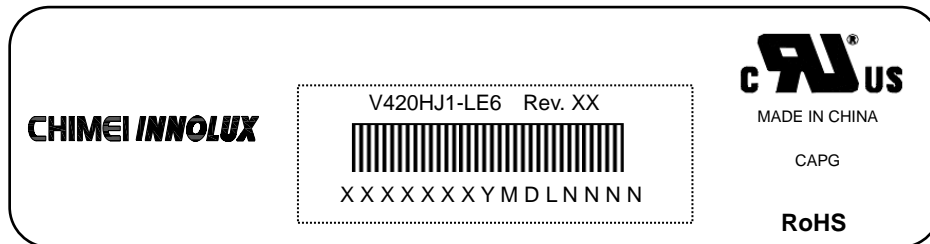
8.2 SAFETY PRECAUTIONS

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [3] After the module's end of life, it is not harmful in case of normal operation and storage.

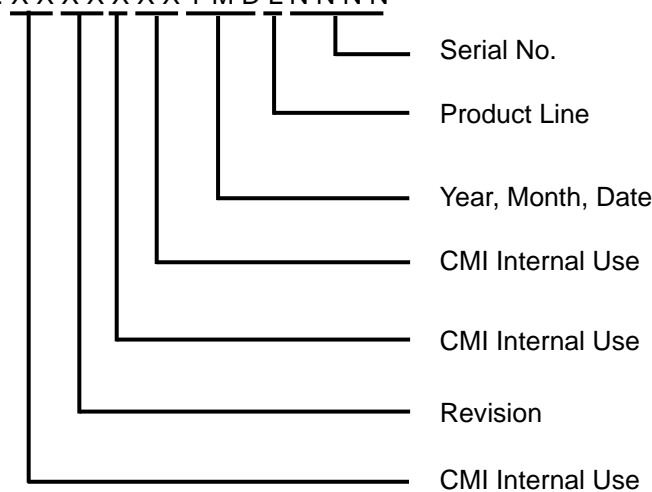
9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V420HJ1-LE6
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 → Line1, 2 → Line 2, ...etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

- (1) 6 LCD TV modules / 1 Box
- (2) Box dimensions : 1085(L)x296(W)x653(H)mm
- (3) Weight : Approx. 50 Kg (6 modules per carton)

10.2 PACKAGING METHOD

Packaging method is shown as following figures.

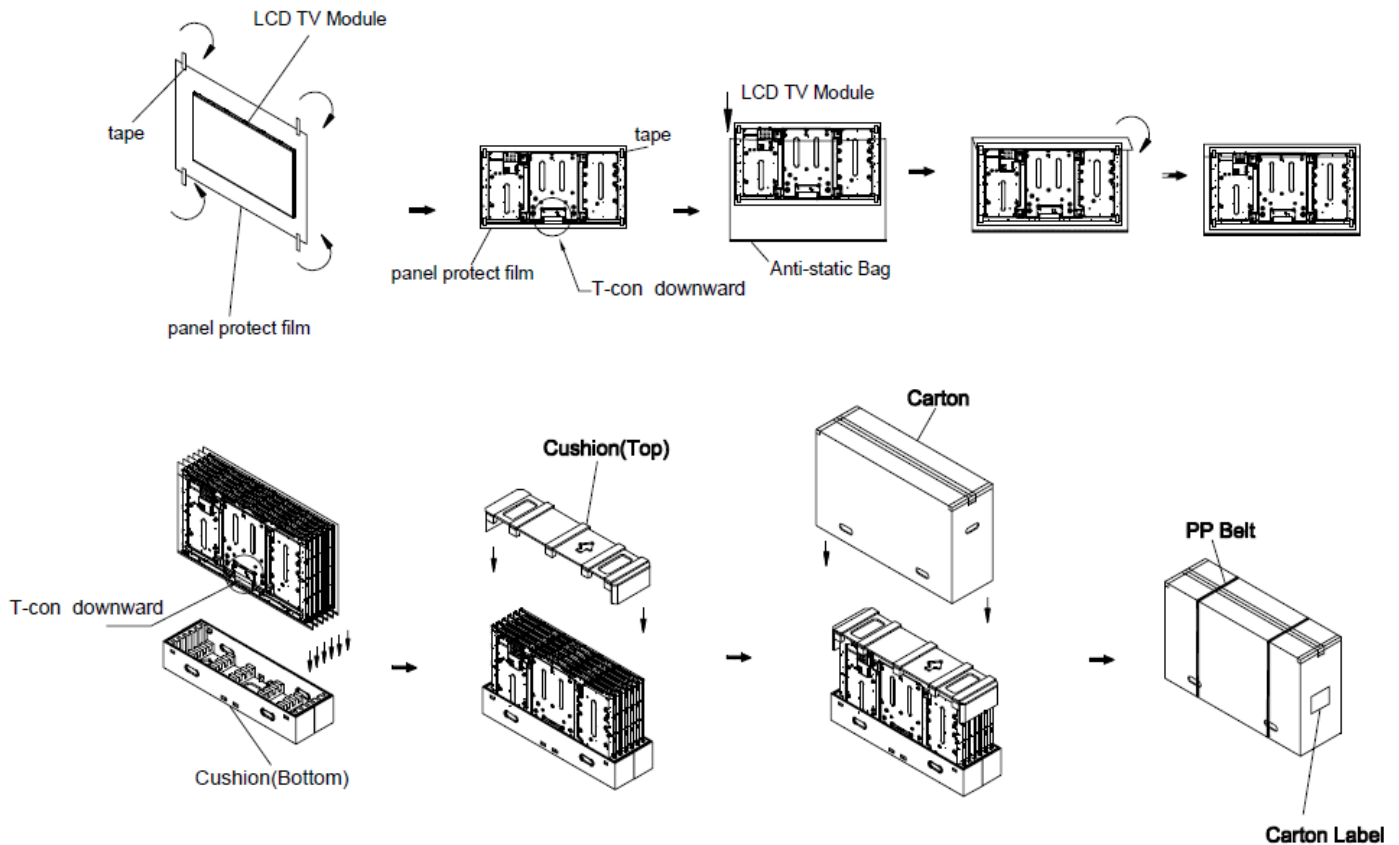


Figure.10-1 packing method

Sea / Land Transportation (40ft & 40ft HQ Container)

Air Transportation

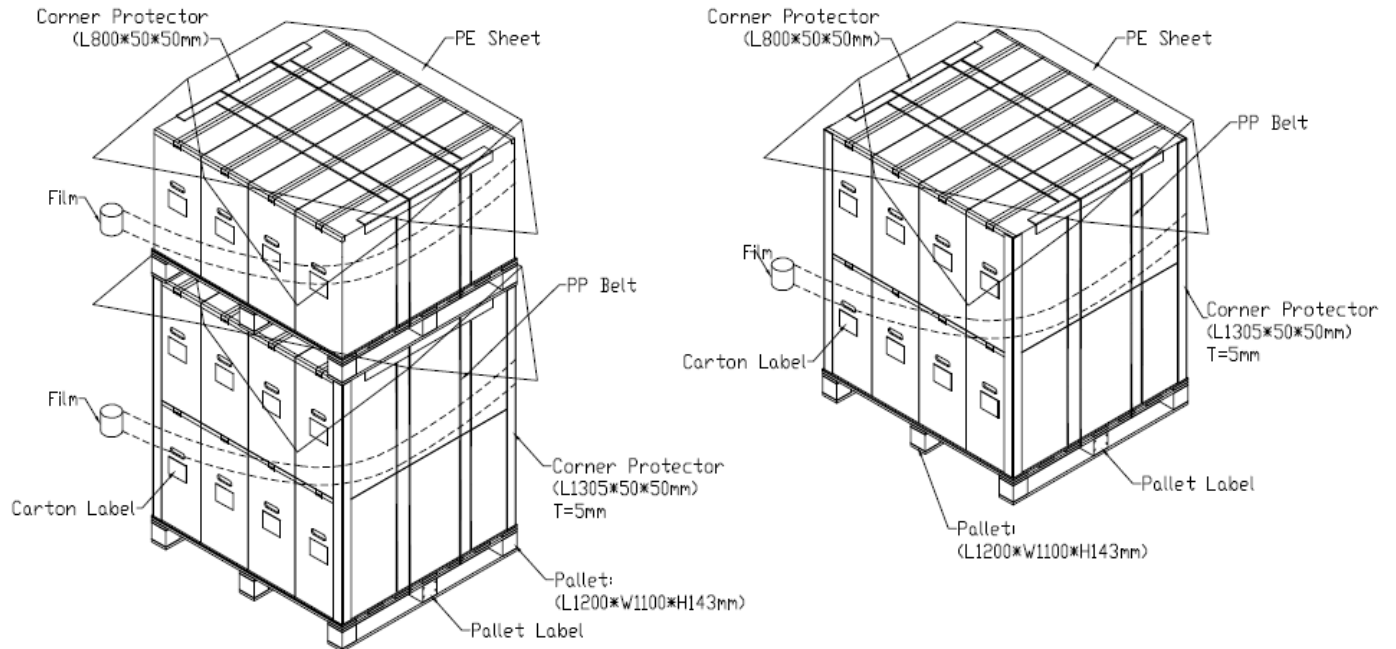


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTIC

